

INPUT STAGE WITH SWITCHED CAPACITORS FOR ANALOG-DIGITAL CONVERTERS.

BACKGROUND OF THE INVENTION

Field of the Invention

5 The present invention refers to an input stage with switched capacitors for analog-digital converters.

Description of the Related Art

Switched capacitor (SC) circuit structures used in analog-digital converters are generally known. The switched capacitor structures used for
10 sampling an analog signal must have a greater sampling rate than the bandwidth of the signal that has to be converted. Said SC structures may be analog input structures of the analog-digital converters.

Figure 1 shows an input circuit structure for an analog-digital converter. Said structure 90 is a switched capacitor structure comprising a first
15 switch 1 connected on one side to a terminal Io on which the analog input signal Vin is present and on the other side connected to an armature A of capacitor Ci, a switch 2 positioned between the same armature A of the capacitor Ci and a reference voltage Vref1, a switch 3 positioned between the armature B of the capacitor Ci and another reference voltage Vref2, a switch 4 connected to the
20 armature B and to a next stage of the analog-digital converter. The switches 1-4 are controlled by the signals f1 and f2 shown in Figure 2; more precisely the switches 1 and 3 are controlled by the signal f1 and the switches 2 and 4 are controlled by the signal f2. The dimension of the capacitor Ci, the conductance during the ignition phase of the switches and the sampling period T determine the
25 dynamic impedance of the structure. The rapid transient of the signal that passes through the elements of the structure 90 causes high current peaks, also called

spikes, that can cause problems in the different applications in which said structure is used, for example problems of interfacing with devices on different chips. For this reason the driving stage of said circuit structure has to be carefully designed as in the case of high resolution analog-digital converters (more than 16 bit); in fact, in the latter, the design of said driving stage becomes more and more critical as it may worsen the performances of the converter itself.

Several solutions have been made for this aim.

One way for not having current spikes is to add an input buffer 10 to the structure 90 of Figure 1 which has the aim of loading it, as shown in Figure 3.

10 The buffer should have a large bandwidth to guarantee a good regulation of the level of the input signal. This buffer represents an expensive solution in terms of area and power consumption and in addition it introduces noise that could worsen the performances of the entire converter.

Another solution consists of using a further switched capacitor structure 100 to reduce the ignition resistance of the structure 90 of Figure 1, as can be seen in Figure 4. The structure 100 is suitable for driving the switch 1 of the circuit structure of Figure 1 that, in Figure 4, is represented by a MOS transistor M. The structure 100 comprises the switches 101-103 driven by the signal f2, the switches 104 and 105 driven by the signal f1 and a capacitor Cb.

15 The switch 101 is positioned between the first terminal of the capacitor Cb and the analog signal Vin while the switch 104 is positioned between said first terminal of the capacitor Cb and the gate terminal of the MOS transistor M. The switch 102 is positioned between the second terminal of the capacitor Cb and ground while the capacitor 105 is positioned between said second terminal of the capacitor Cb and a voltage Vdd; the switch 103 is positioned between the gate terminal of the transistor M and ground. The closing of the switches 101-103 permits the capacitor Cb to be loaded at the voltage Vin and to unload the intrinsic capacitances of the transistor M linked to the drain terminal. The successive closing of the switches 104 and 105 enables the MOS transistor M to be driven

with a voltage between gate terminal and source terminal equal to V_{dd} since on the gate terminal the voltage $V_{dd}+V_{in}$ is present. Said structure 100 guarantees good linearity of the signal in the input structure but the reduction of the ignition resistance causes an increase of the current spikes in input to the structure of

5 Figure 1.

A further solution is constituted by a capacitive sampling circuit shown in Figure 5. Said circuit is similar to the circuit of Figure 3 in which a switch 11 positioned between the input terminal IN of the buffer 10 and the terminal A of the capacitor C_i has been added. The switches 1 and 11 therefore become the
10 first sampling switches of the structure 90; in fact they are controlled by the signals f_{1a} and f_{1b} shown in Figure 6 that come from the signal f_1 and which both contribute to loading the capacitor C_i up to the voltage level V_{in} . More precisely considering T as the sampling period, the first semi-sampling period $T/2$ is divided into two more semi-periods $T/4$; in the first period $T/4$ the signal f_{1a} is positive and
15 thus the switch 1 is active, while in the second period $T/4$ the signal f_{1b} is positive and the switch 11 becomes active. With this solution the noise introduced by the buffer does not invalidate the performances of the converter as said buffer is disconnected during the second period $T/4$.

BRIEF SUMMARY OF THE INVENTION

20 One embodiment of the present invention provides an input stage with switched capacitors for analog-digital converters, which is able to improve the linearity and reduce the current spikes more than the input stages known.

One embodiment of the present invention provides an input stage with switched capacitors for analog-digital converters, the stage including a first
25 switched capacitor circuit structure suitable for sampling an analog signal in input to the converter with un preset sampling period, a buffer having in input the analog signal and being connectable to the first circuit structure by means of a first and a second sampling switch of the first circuit structure coupled respectively with the

output terminal and the input terminal of the buffer, the first and second switch being controlled respectively by a first and a second signal to close respectively for a first interval of time and for a successive second interval of time of a first semi-sampling period of the analog signal, characterised in that it comprises a second
5 switched capacitor circuit structure connected to a reference voltage and a the buffer and suitable for generating the second signal with a voltage value greater in absolute value than the value of the analog signal for the duration of the second interval of time of the semi-sampling period.

BRIEF DESCRIPTION OF THE DRAWINGS

10 The characteristics and advantages of the present invention will appear evident from the following detailed description of an embodiment thereof, illustrated as a non-limitative example in the enclosed drawings, in which:

 Figure 1 is a schematic view of a switched capacitor circuit structure used as input stage for a analog-digital converter according to the known art;

15 Figure 2 is a graph of the control signals of the switches of Figure 1 in function of the time;

 Figure 3 is a schematic view of another switched capacitor circuit structure used as input stage for an analog-digital converter according to the known art;

20 Figure 4 is a schematic view of a further switched capacitor circuit structure used as input stage for an analog-digital converter according to the known art;

 Figure 5 is a schematic view of a further switched capacitor circuit structure used as input stage for an analog-digital converter according to the
25 known art;

 Figure 6 is a graph of the control signals of several switches of Figure 1 in function of the time;

Figure 7 is a schematic view of a switched capacitor circuit structure used as input stage for an analog-digital converter according to an embodiment of the present invention;

Figure 8 is a schematic view of a switched capacitor circuit structure
5 used as input stage for an analog-digital converter according to an alternate embodiment of the present invention;

Figure 9 is a time diagram of the current in input to the circuit structure of Figure 1;

Figure 10 is a time diagram of the current in input to the circuit
10 structure of Figure 8.

DETAILED DESCRIPTION OF THE INVENTION

With reference to Figure 7 description is made of an input stage with switched capacitors for analog-digital converters according to one embodiment of the present invention; the circuit elements already previously described will be
15 indicated with the same numerical references. Said stage comprises a first switched capacitor structure 200 suitable for sampling the analog signal V_{in} in input to the analog-digital converter and a buffer 10 that has in input said analog signal V_{in} and the output terminal OUT connected to the circuit structure 200. The latter has two first sampling switches 1 and 11 driven by the f_{1a} and F so as to be
20 alternatively active in a half $T/4$ of the semi-sampling period $T/2$ of the analog signal V_{in} , that is respectively for a first and for a successive second interval of time $T/4$. The switches 1 and 11 are connected respectively with the output terminal OUT and input terminal IN of the buffer 10. The switch 11 is preferably constituted by a MOS transistor M1 on whose gate terminal G the driving signal F
25 coming from a circuitry 50 lies. The latter is connected between the input terminal IN of the buffer 10 and the gate terminal of the transistor 11 and comprises a capacitor C1 having a terminal A1 that can be connected to the input terminal IN of the buffer 10 by means of a switch 51 and a terminal B1 that can be connected to

the gate terminal of the transistor 11 by means of a switch 54; the signal f1b of Figure 6 lies on the switches 51 and 54. The switches 52, 53 and 55 are driven by the signal f2 and respectively the switch 52 is positioned between the terminal A1 of the capacitor C1 and ground, the switch 53 is positioned between the terminal B2 of the capacitor C1 and a reference voltage Vdd, and the switch 55 is positioned between the gate terminal G of the transistor 11 and ground.

When the signal f2 is positive the switches 52, 53 and 55 are closed and this permits the loading of the capacitor C1 at the voltage Vdd and the unloading of the intrinsic capacities of the transistor 11 connected to the gate terminal; the signal F in said semi-period is at ground. When the signal f1b is positive, that is in the second interval of time $T/4$, the switches 51 and 54 are closed. In this manner we obtain on the gate terminal G of the transistor 11 a driving signal in voltage F greater in absolute value than the value of the voltage Vin; in this case a signal F on the gate terminal G equal to $V_{dd} + V_{in}$, that is a voltage between gate and source equal to Vdd that permits the switch 11 to be closed.

The use of a gate-source voltage equal to Vdd reduces the ignition resistance of the transistor 11 which is translated in a lower distortion of the signal that passes through the transistor 11.

It can be appreciated that the signal f1 is positive during the entire first semi-sampling period $T/2$ such that the switch 3 of the switched capacitor structure 200 is closed, while the switch 1 is closed by the signal f1a in the first interval $T/4$, and the switch 11 is closed by the signal f1a in the second interval $T/4$. When the signal f2 is positive during the entire second semi-sampling period $T/2$, the switches 2, 4 of the first switched capacitor structure 200 are closed along with the switches 52, 53, 55 of the second switched capacitor structure 50.

Figure 8 shows an input stage with switched capacitors for analog-digital converters according to an alternate embodiment of the present invention. In this variation the circuitry 50 for driving the transistor 11, in a different manner

from the embodiment described in Figure 7, is directly connected with the output terminal OUT of the buffer 10 instead of with the input terminal IN. In this manner the buffer 10 is used during the phase f1b to load the capacitor C1 of the circuitry 50 and the intrinsic capacitances to the MOS transistor 11 (shown in a dotted line in Figure 8), that is the capacitance between gate and drain Cgd, the capacitance between gate and source Cgs and the capacitance between gate and substrate Cgb (which is normally connected between gate and ground but for the calculation of the total capacitance is shown in parallel with the capacitance Cgs). The total load capacitance CL that the buffer 10 has to load is given by

$$CL = \frac{C1 * (Cgd + Cgs + Cgb)}{C1 + Cgd + Cgb + Cgs}$$

In this manner the input source that sends the signal Vin has to load a reduced capacitive load in comparison to the circuit of Figure 7 and given exclusively by the sampling capacitor Ci; this permits the reduction of the current spikes.

Figures 9 and 10 show time diagrams of the currents I1 and I2 on the input terminals Io and IN respectively of the circuitry typology of Figure 1 and of that of Figure 8 using a capacitor Ci = 4.7 pF, a capacitor C1 = 2 pF and a buffer having a gain in voltage equalling 50db and a frequency band of 400Mhz. The diagram of Figure 9 shows an input current I1 with variations between a positive peak and a negative peak of current greater than 20 mA, while the diagram of Figure 10 shows an input current I2 with variations between a positive peak and a negative peak of current less than 2 mA. For the circuit typology of Figure 7, even if it is not shown with a time diagram, a current on the input terminal IN is also obtained with variations between a positive peak and a negative peak of current of about 2.7 mA.

All of the above U.S. patents, U.S. patent application publications, U.S. patent applications, foreign patents, foreign patent applications and non-

patent publications referred to in this specification and/or listed in the Application Data Sheet, are incorporated herein by reference, in their entirety.

- From the foregoing it will be appreciated that, although specific embodiments of the invention have been described herein for purposes of illustration, various modifications may be made without deviating from the spirit and scope of the invention. Accordingly, the invention is not limited except as by the appended claims.
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